What is claimed is:

1. An integrated circuit structure which comprises a substrate and

(a) an inorganic layer on the substrate which comprises a pattern of metal lines on the substrate and an inorganic dielectric on the substrate between the metal lines; and

(b) an organic layer on the inorganic layer which comprises an organic dielectric having metal filled vias therethrough which connect to the metal lines of the inorganic layer.

2. The integrated circuit structure of claim 1 which comprises

(c) an additional inorganic layer on the organic layer which comprises a pattern of additional metal lines on the organic layer and an inorganic dielectric on the organic layer between the additional metal lines; and

(d) an additional organic layer on the additional inorganic layer which comprises an organic dielectric having metal filled vias therethrough which connect to the additional metal lines of the additional inorganic layer.

3. The integrated circuit structure of claim 2 which comprises one or more further alternating inorganic layers (c) and organic layers(d) on the additional inorganic layer (c) and organic layer (d).

4. The integrated circuit structure of claim 2 further comprising an inorganic dielectric layer on the organic layer between the vias and under the additional metal lines of the additional inorganic layer; and an organic dielectric on the inorganic dielectric layer between the additional metal lines of the additional inorganic layer.

5. The integrated circuit structure of claim 3 further comprising an inorganic dielectric layer on each alternating organic layer (d) between the vias and under the additional metal lines of the alternating inorganic layer; and an organic dielectric on

the inorganic dielectric layer between the additional metal lines of the additional inorganic layer.

6. The integrated circuit structure of claim 1 wherein the metal lines and vias have a barrier metal on one or more edges thereof.

7. A process for producing an integrated circuit structure which comprises

(a) providing a substrate which comprises a pattern of metal lines on the substrate and a dielectric on the substrate between the metal lines;

(b) depositing an organic dielectric layer on the substrate;

(c) depositing an inorganic dielectric layer on the organic dielectric;

(d) etching a pattern of vias through the inorganic dielectric layer;

(e) etching a pattern of vias through the organic dielectric layer which correspond to the pattern of vias through the inorganic dielectric layer;

(f) applying a photoresist to the top of the inorganic dielectric layer and filling the vias in the organic dielectric layer and the inorganic dielectric layer with photoresist;

(g) imagewise removing a portion of the photoresist from the top of the inorganic dielectric layer; and removing a portion and leaving a portion of the photoresist through a thickness of the inorganic dielectric layer;

(h) removing part of the inorganic dielectric layer underlying the portions of the photoresist removed from the top of the inorganic dielectric layer to form trenches in the inorganic dielectric layer;

(i) removing the balance of the photoresist from the top of the inorganic dielectric layer and from the vias;

(j) filling the vias in the organic dielectric and the trenches in the inorganic dielectric with a metal.

8. The process of claim 7 wherein steps (b) through (j) are repeated at least once on the previously formed integrated circuit structure.

9. The integrated circuit structure produced according to the process of claim 7.

10. The integrated circuit structure produced according to the process of claim 8.

11. A process for producing an integrated circuit structure which comprises

(a) providing a substrate, which comprises a pattern of metal lines on the substrate and a dielectric on the substrate between the metal lines;

(b) depositing an organic via level dielectric on the substrate;

(c) depositing an thin inorganic dielectric layer on the organic via level dielectric;

(d) imagewise patterning and removing a portion of the thin inorganic dielectric layer thus defining vias through the thin inorganic dielectric layer;

(e) depositing a thin organic dielectric etchstop material layer on the thin inorganic dielectric layer and filling the vias in the thin inorganic dielectric layer with the organic dielectric material;

(f) depositing a metal level inorganic dielectric layer on the organic dielectric etchstop layer;

(g) imagewise patterning and removing a portion of the metal level inorganic dielectric layer down to the organic dielectric etchstop material layer to form trenches in the metal level inorganic dielectric layer;

(h) removing the portion of the organic dielectric etchstop material layer underlying the corresponding removed portion of the metal level inorganic dielectric to form trenches therein, and removing the organic etchstop material from the vias in the thin inorganic dielectric layer;

(i) removing the portion of the organic via level dielectric layer underlying the thin inorganic dielectric layer thus forming vias through the organic via level dielectric layer down to the metal lines;

(j) filling the vias in the via level organic dielectric layer and the thin inorganic dielectric layer, and trenches in the organic dielectric etchstop layer and metal level inorganic dielectric layer with a metal.

12. The process of claim 11 wherein steps (b) through (j) are repeated at least once on the previously formed integrated circuit structure.

13. The integrated circuit structure produced according to the process of claim 11.

14. The integrated circuit structure produced according to the process of claim 12.

15. A process for producing an integrated circuit structure which comprises

(a) providing a substrate, which comprises a pattern of metal lines on the substrate and a dielectric on the substrate between the metal lines;

(b) depositing an organic via level dielectric layer on the substrate;

(c) depositing an thin inorganic dielectric layer on the organic via level dielectric;

(d) depositing a thin organic dielectric etchstop material layer on the thin inorganic dielectric layer;

(e) depositing a metal level inorganic dielectric layer on the organic dielectric etchstop layer;

(f) imagewise patterning and removing a portion of the metal level inorganic dielectric layer down to the organic dielectric etchstop material layer to form vias in the metal level inorganic dielectric layer;

(g) removing the portion of the organic dielectric etchstop material layer underlying the corresponding removed portions of the metal level inorganic dielectric layer to form vias in the organic dielectric etchstop material layer;

(h) removing the portion of the thin inorganic dielectric layer underlying the corresponding removed portions of the organic dielectric etchstop material layer to form vias in the thin inorganic dielectric layer;

(i) covering the top of the metal level inorganic dielectric layer with a photoresist and filling the vias in the metal level inorganic dielectric layer, the organic dielectric etchstop material layer and the thin inorganic dielectric layer with photoresist;

(j) imagewise patterning and removing a portion of the photoresist from the top of the metal level inorganic dielectric layer; and removing a portion and leaving a portion of the photoresist through a thickness of the metal level inorganic dielectric layer;

(k) removing part of the metal level inorganic dielectric layer underlying the portions of the photoresist removed from the top of the inorganic dielectric layer to form trenches in the metal level inorganic dielectric layer;

(l) removing the balance of the photoresist from the top of the metal level inorganic dielectric layer and from the vias; and removing the portion of the organic dielectric etchstop material layer underlying the trenches until the thin inorganic dielectric layer is reached;

(m) removing the portion of the organic via level dielectric layer underlying the vias in the thin inorganic dielectric layer;

(n) filling the vias in the via level organic dielectric layer and the thin inorganic dielectric layer, and trenches in the organic dielectric etchstop layer and metal level inorganic dielectric layer with a metal.

16. The process of claim 15 wherein steps (b) through (n) are repeated at least once on the previously formed integrated circuit structure.

17. The integrated circuit structure produced according to the process of claim 15.

18. The integrated circuit structure produced according to the process of claim 16.

19. A process for producing an integrated circuit structure which comprises

(a) providing a substrate, which comprises a pattern of metal lines on the substrate and a dielectric on the substrate between the metal lines;

(b) depositing an organic via level dielectric layer on the substrate;

(c) depositing an thin inorganic dielectric layer on the organic via level dielectric

(d) depositing a thin organic dielectric etchstop material layer on the thin inorganic dielectric layer;

(e) depositing a metal level inorganic dielectric layer on the organic dielectric etchstop layer;

(f) imagewise patterning and removing a portion of the metal level inorganic dielectric layer down to the organic dielectric etchstop material layer to form vias in the metal level inorganic dielectric layer;

(g) removing the portion of the organic dielectric etchstop material layer underlying the corresponding removed portions of the metal level inorganic dielectric layer to form vias in the organic dielectric etchstop material layer;

(h) removing the portion of the thin inorganic dielectric layer underlying the corresponding removed portions of the organic dielectric etchstop material layer to form vias in the thin inorganic dielectric layer;

(i) removing the portion of the organic via level dielectric layer underlying the corresponding removed portions of the thin inorganic dielectric layer to form vias in the organic via level dielectric layer;

(j) covering the top of the metal level inorganic dielectric layer with a photoresist and filling the vias in the metal level inorganic dielectric layer, the organic dielectric etchstop material layer, the thin inorganic dielectric layer and the organic via level dielectric layer with photoresist;

(k) imagewise patterning and removing a portion of the photoresist from the top of the inorganic dielectric layer; and removing a portion and leaving a portion of the photoresist through a thickness of the metal level inorganic dielectric layer;

(l) removing part of the metal level inorganic dielectric layer underlying the portions of the photoresist removed from the top of the inorganic dielectric layer to form trenches in the metal level inorganic dielectric layer;

(m) removing the balance of the photoresist from the top of the metal level inorganic dielectric layer and from the vias; and removing the portion of the organic dielectric etchstop material layer underlying the trenches until the thin inorganic dielectric layer is reached;

(n) filling the vias in the via level organic dielectric layer and the thin inorganic dielectric layer, and trenches in the organic dielectric etchstop layer and metal level inorganic dielectric layer with a metal.

20. The process of claim 15 wherein steps (b) through (n) are repeated at least once on the previously formed integrated circuit structure.

21. The integrated circuit structure produced according to the process of claim 19.

22. The integrated circuit structure produced according to the process of claim 20.

23. An integrated circuit structure which comprises a substrate and
(a) an organic layer on the substrate which comprises a pattern of metal lines on the substrate and an organic dielectric on the substrate between the metal lines; and
(b) an inorganic layer on the organic layer which comprises an inorganic dielectric having metal filled vias therethrough which connect to the metal lines of the organic layer.

24. The integrated circuit structure of claim 23 which comprises
(c) an additional organic layer on the inorganic layer which comprises a pattern of additional metal lines on the inorganic layer and an organic dielectric on the inorganic layer between the additional metal lines; and
(d) an additional inorganic layer on the additional organic layer which comprises an inorganic dielectric having metal filled vias therethrough which connect to the additional metal lines of the additional organic layer.

25. The integrated circuit structure of claim 24 which comprises one or more further alternating organic layers (c) and inorganic layers (d) on the additional organic layer (c) and inorganic layer (d).

26. The integrated circuit structure of claim 24 further comprising an organic dielectric layer on the inorganic layer between the vias and under the additional metal lines of the additional organic layer; and an inorganic dielectric on the organic dielectric layer between the additional metal lines of the additional organic layer.

27. The integrated circuit structure of claim 25 further comprising an organic dielectric layer on each alternating inorganic layer (d) between the vias and under the additional metal lines of the alternating organic layer; and an inorganic dielectric on the organic dielectric layer between the additional metal lines of the additional organic layer.

28. The integrated circuit structure of claim 23 wherein the metal lines and vias have a barrier metal on one or more edges thereof.

29. A dielectric coated substrate which comprises:
(a) a first dielectric composition film on a substrate; and
(b) a second dielectric composition film on the first dielectric composition film;
wherein the first dielectric composition and the second dielectric composition have substantially different etch resistance.

30. The dielectric coated substrate of claim 29 wherein the first dielectric composition film is organic and the second dielectric composition film is inorganic.

31. The dielectric coated substrate of claim 29 wherein the first dielectric composition film is inorganic and the second dielectric composition film is organic.